EXAMINER'S AMENDEMENT

1. . An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Lois D Cartier (Reg. No. 40941) on 03 March 2010.

3. The claims had been amended as follows:

1. (Currently amended) A method for multithread processing of messages using an integrated circuit, comprising:

configuring configurable logic of said integrated circuit to have a plurality of thread circuits and an interconnection topology amongst said plurality of thread circuits, each of said plurality of thread circuits comprising a state machine and providing a control signal to each other of said plurality of thread circuits through said interconnection topology;

concurrently processing messages using said plurality of thread circuits; ~~and~~

controlling operation of at least one thread circuit of said plurality of thread circuits in accordance with control data of a respective control signal from at least one other thread circuit of said plurality of thread circuits over said interconnection topology by at least one of activating, deactivating, or suspending said at least one thread circuit in response to said control data, wherein said control data comprises status data associated with said at least one other thread circuit of said plurality of thread circuits; and

communicating data from a first thread circuit of said plurality of thread circuits to a second thread circuit of said plurality of thread circuits through said interconnection topology.

2. (Canceled)

3. (Proposed Amendment) The method of claim [[2]] 1, wherein said integrated circuit is a programmable device, and wherein said state machine of each of said plurality of thread circuits is implemented using programmable blocks of said integrated circuit.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Currently amended) A method of implementing multithread processing of messages using an integrated circuit, comprising:

specifying a plurality of threads each comprising a state machine for concurrently processing messages, at least one thread of said plurality of threads including control logic for controlling operation of at least one other thread of said plurality of threads by at least one of starting, stopping, or suspending of said at least one other thread;

specifying an interconnection topology amongst said plurality of threads, at least a portion of said interconnection topology including a first connection between said at least one thread and said at least one other thread and a second connection for communicating data from a first thread of said plurality of threads to a second thread of said plurality of threads, said first connection including at least one control signal provided by said control logic; and

generating a physical description of a multithreading system in response to said plurality of threads and said interconnection topology, said physical description being defined in terms of components of said integrated circuit.

8. (Original) The method of claim 7, further comprising:

processing said physical description to generate data for configuring said integrated circuit with said multithreading system.

9. (Original) The method of claim 8, wherein said physical description comprises a hardware description language description.

10. (Canceled)

11. (Canceled)

12. (Currently amended) The method of claim [[11]] 7, wherein said data is communicated in accordance with a data validity flag.

13. (Currently amended) The method of claim [[11]] 7, wherein said data is communicated in accordance with a request generated by said second thread.

14. (Previously Presented) A design tool for implementing a multithread message processing system using an integrated circuit, comprising:

~~means for specifying attributes of said multithread message processing system;~~

~~a first database for storing a multithread model having a thread model and an interconnection model;~~

~~a second database for storing an architecture of said integrated circuit; and~~

~~a multithread model section, comprising:~~

~~means for generating a plurality of instances of said thread model and an instance of said interconnection model in response to said specified attributes; and~~

~~means for implementing said plurality of thread model instances and said interconnection model instance in terms of said integrated circuit architecture~~

means for specifying a plurality of threads each comprising a state machine for concurrently processing messages, at least one thread of said plurality of threads including control logic for controlling operation of at least one other thread of said plurality of threads by at least one of starting, stopping, or suspending of said at least one other thread;

means for specifying an interconnection topology amongst said plurality of threads, at least a portion of said interconnection topology including a first connection between said at least one thread and said at least one other thread and a second connection for communicating data from a first thread of said plurality of threads to a second thread of said plurality of threads, said first connection including at least one control signal provided by said control logic; and

means for generating a physical description of a multithreading system in response to said plurality of threads and said interconnection topology, said physical description being defined in terms of components of said integrated circuit.

15. (Canceled)

16. (Canceled)

17. (Currently amended) The design tool of claim [[16]] 14, wherein said integrated circuit is a programmable device, and where said state machine associated with each of said plurality of threads ~~thread model instances~~ is implemented using programmable blocks of said programmable device.

18. (Currently amended) An apparatus for multithread processing of messages using an integrated circuit, comprising:

a first configured portion within said integrated circuit for concurrently processing messages using a plurality of thread circuits each comprising a state machine, wherein at least one of said plurality of thread circuits ~~having~~ includes control logic for controlling operation of at least one other thread circuit of said plurality of thread circuits by at least one of activating, deactivating, or suspending said at least one other thread circuit in response to control data from the at least one thread circuit, and wherein a first thread circuit of said plurality of thread circuits is configured to communicate data to a second thread circuit of said plurality of thread circuits; and

a second configured portion within said integrated circuit for providing a first connection between said at least one thread and said at least one other thread and a second connection between said first and second thread circuits, said first connection including at least one control signal provided by said control logic that provides said control data.

19. (Previously Presented) The apparatus of claim 18, wherein said integrated circuit is a programmable device.

20. (Canceled).

Allowable Subject Matter

4. Claims **1, 3, 7-9, 12-14 and 17-19** are allowed.

5. The following is an examiner's statement of reasons for allowance:

The arts of record used as the basis for the previous rejection, He et al (US 20020120912), Ohnishi(U.S 20020188923), and Weber et al (US 20020129173) do

not expressly teach or render obvious the invention as recited in independent **claims 1 and 7, 14 and 18.**

a. As to **claim 1**, the art of record does not expressly teach each of said plurality of thread circuits comprising a state machine and providing a control signal to each other of said plurality of thread circuits through said interconnection topology; concurrently processing messages using said plurality of thread circuits; controlling operation of at least one thread circuit of said plurality of thread circuits in accordance with control data of a respective control signal from at least one other thread circuit of said plurality of thread circuits over said interconnection topology by at least one of activating, deactivating, or suspending said at least one thread circuit in response to said control data, wherein said control data comprises status data associated with said at least one other thread circuit of said plurality of thread circuits; and communicating data from a first thread circuit of said plurality of thread circuits to a second thread circuit of said plurality of thread circuits through said interconnection topology; when taken in the context of the claim, as a whole. More over, the art of record does not provide a basis of evidence for asserting a motivation driven from the art or from one knowledgeable in the art, that one of ordinary skill in the art at the time the invention was made would have modified the method for multithread processing of messages to combine the disclosed limitations as recited in the context of **Claim 1.**

b. As to **claim 7**, the art of record does not expressly teach specifying a plurality of threads each comprising a state machine for concurrently processing messages, at least one thread of said plurality of threads including control logic for controlling operation of at least one other thread of said plurality of threads by at least one of starting, stopping, or suspending of said at least one other thread; specifying an interconnection topology amongst said plurality of threads, at least a portion of said interconnection topology including a first connection between said at least one thread and said at least one other thread and a second connection for communicating data from a first thread of said plurality of threads to a second thread of said plurality of threads, said first connection including at least one control signal provided by said control logic; when taken in the context of the claim, as a whole. More over, the art of record does not provide a basis of evidence for asserting a motivation driven from the art or from one knowledgeable in the art, that one of ordinary skill in the art at the time the invention was made would have modified the method of implementing multithread processing of messages to combine the disclosed limitations as recited in the context of **Claim 7.**

c. As to **Claim 14,** being directed to system for implementing a multithread message processing having substantially the same limitations as **Claim 7 ,** this claim is allowable for the same reasoning as recited in **Claim 7** above.

d. As to **Claim 18,** being directed to system for multithread processing of messages having substantially the same limitations as **Claim 1,** this claim is allowable for the same reasoning as recited in **Claim 1** above.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdou Karim Seye whose telephone number is 571-270-1062. The examiner can normally be reached on Monday - Friday 8:30 - 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sough Hyung can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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